AUTO CHARGE INTERLOCK / A04 MATERIALS / SCHEMATIC CANDIDATE

J1
RAW_5V 1
GND 2
CE 3
RAW_5V
GND
CE
4755 RAW/GND/CE

J2
NTC 1
GND 2
TH2
GND
TH2 103AT-2

J3
WINDOW_OK 1
GND 2
WINDOW_OK
GND
INHIBIT short to stop

J4
ALLOW 1
GATE_SOURCE 2
ALLOW
GATE_SOURCE
ARM default OPEN

U1
VREF 1
GND 2
VREF 3
K
A
REF
TL431ILP

U2
WINDOW_OK 1
NTC 2
COLD 3
RAW_5V 4
NTC 5
HOT 6
WINDOW_OK 7
WINDOW_OK 8
REF_LOW 9
VREF 10
GND 11
REF_HIGH 12
VREF 13
WINDOW_OK 14
OUTA
INA−
INA+
VCC
INB+
INB−
OUTB
OUTC
INC−
INC+
VEE
IND+
IND−
OUTD
TLV7044PWR

U3
WINDOW_OK 1
NOT_READY 2
NOT_READY 3
ALLOW 4
GND 5
GND 7
GND 9
GND 11
GND 13
RAW_5V 14
1A
1Y
2A
2Y
3A
3Y
GND
4Y
4A
5Y
5A
6Y
6A
VCC
SN74HC14D

U4
GATE 1
GND 2
MR_LOCAL 3
CT 4
UV_SENSE 5
RAW_5V 6
RESET_N
GND
MR
CT
SENSE
VDD
TPS3808G01DBVR

Q1
GATE 1
GND 2
CE 3
G
S
D
AO3400A

R1
RAW_5V 1
VREF 2
RAW_5V
VREF
1k 1%

R2
VREF 1
NTC 2
VREF
NTC
10k 1%

R3
VREF 1
COLD 2
VREF
COLD
10k 1%

R4
COLD 1
GND 2
COLD
GND
17.8k 1%

R5
VREF 1
HOT 2
VREF
HOT
10k 1%

R6
HOT 1
GND 2
HOT
GND
6.98k 1%

R7
RAW_5V 1
REF_LOW 2
RAW_5V
REF_LOW
30k 1%

R8
REF_LOW 1
GND 2
REF_LOW
GND
10k 1%

R9
RAW_5V 1
REF_HIGH 2
RAW_5V
REF_HIGH
10k 1%

R10
REF_HIGH 1
GND 2
REF_HIGH
GND
30k 1%

R11
RAW_5V 1
WINDOW_OK 2
RAW_5V
WINDOW_OK
4.7k 1%

R13
RAW_5V 1
CT 2
RAW_5V
CT
100k 1%

R14
RAW_5V 1
UV_TOP 2
RAW_5V
UV_TOP
100k 0.1%

R15
UV_TOP 1
UV_SENSE 2
UV_TOP
UV_SENSE
499R 0.1%

R16
UV_SENSE 1
GND 2
UV_SENSE
GND
10k 0.1%

R17
GATE_SOURCE 1
GATE 2
GATE_SOURCE
GATE
10k 1%

R18
GATE 1
GND 2
GATE
GND
100k 1%

C1
RAW_5V 1
GND 2
RAW_5V
GND
100nF X7R 50V

C2
RAW_5V 1
GND 2
RAW_5V
GND
100nF X7R 50V

C3
RAW_5V 1
GND 2
RAW_5V
GND
100nF X7R 50V

C4
UV_SENSE 1
GND 2
UV_SENSE
GND
1nF X7R 50V

TP1
RAW_5V 1
RAW_5V
RAW

TP2
VREF 1
VREF
REF

TP3
NTC 1
NTC
NTC

TP4
WINDOW_OK 1
WINDOW_OK
WIN

TP5
GATE 1
GATE
GATE analog

TP6
CE 1
CE
CE

TP7
GND 1
GND
GND

H1
M3 NPTH

H2
M3 NPTH

H3
M3 NPTH

H4
M3 NPTH

R19
MR_LOCAL 1
GND 2
MR_LOCAL
GND
22k 1%

R21
WINDOW_OK 1
MR_LOCAL 2
WINDOW_OK
MR_LOCAL
100R 1%

R20
RAW_5V 1
CE 2
RAW_5V
CE
1k PERMANENT ON 4755

R34
CE 1
GND 2
CE
GND
10k EXISTING ON 4755

#FLG01
RAW_5V 1
PWR
SELV source RAW_5V

#FLG02
GND 1
PWR
SELV source GND

Typed pins and package numbers. R20 stays on charger side; R34 is existing. J4 default OPEN.

J1 carries RAW5V/GND/CE control only. Do not directly parallel ESP32 USB 5V and backup boost output.

TPS3808G01 senses RAW5V and WINDOW_OK: recovery nominal 300ms (180..420ms datasheet). No field release.

No battery or hardware tests yet. Single-fault and thermal attachment verification remain mandatory.

Prototype design: fabrication / unattended field release HOLD

Sheet: /
File: CG-AUTOCHG-EVT1.kicad_sch

Title: ColdGuard autocharge interlock EVT1

Size: A2	Date: 2026-10-06	**Rev: EVT1-A04**
KiCad E.D.A. 10.0.6		Id: 1/1